TEXAS INSTRUMENTS
INCORPORATED

TMS 9929A

EUROPEAN LINE FORMAT

VIDEO DISPLAY PROCESSOR

PRELIMINARY DATA

Prepared by: Carlo Herrmann

March 24, 1980

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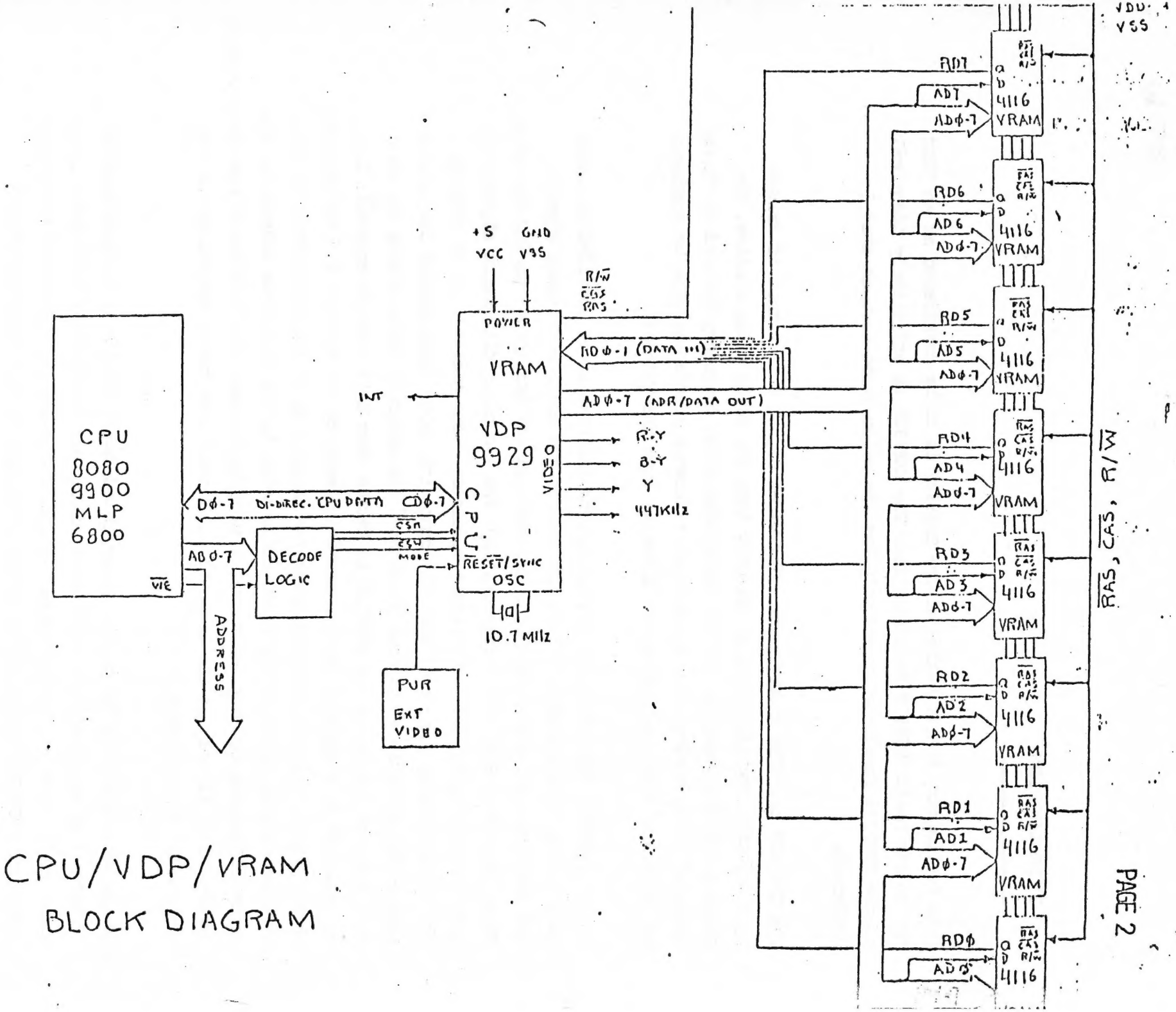
INTRODUCTION

This Preliminary Specification of the TMS9929 is to be considered as an "ADD ON" to the basic TMS9918 specification. The TMS9929 is effectively identical to the TMS9918 functionally and only has the color video section that is different.

The TMS9918 provides a composite color video signal output that if driven by a suitable amplifier can go directly into any color video monitor. The color burst frequency is the VDP oscillator input frequency divided by three. External video mixing with an external reference source can also be achieved by inputting this external source directly into the TMS9918.

In the TMS9929 the color and luminance/sync information is provided on three pins rather than a single pin in the form of two color difference signals and one luminance signal with all the vertical and horizontal timing included. So we have R-Y, B-Y, and Y respectively. The two color difference signals are used then by an external quadrature modulator video encoder. It is outside the Video Display Processor that the composite color video signal is generated into a PAL or Secam compatible TV signal. The external video mixing is also done outside and it is the TMS9929 to decide when this mode is entered. This is achieved by a special level distinction made by the R-Y and B-Y VDP outputs. When external video is entered these two outputs go to the equivalent of the sync percentage level of the black-white swing in the luminance output, ie- the color difference outputs are normally swinging between the luminace black-white voltage levels and it is only in the external video mode that these outputs go to the reserved " sync " level.

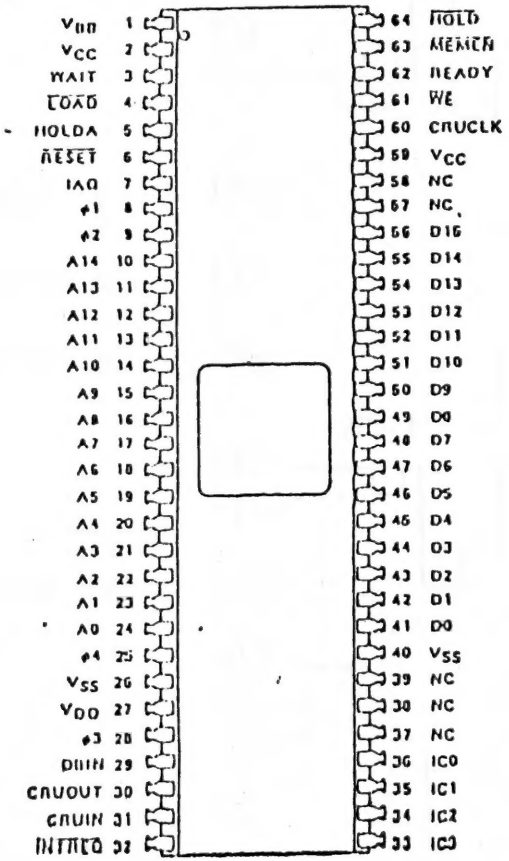
Phase locking of the VDP to the external PAL burst frequency is desirable if inter-hum or crawl effects want to be minimized. The TMS9929 oscillator clock must still, however, be maintained within its prescribed limits of oscillator operation. CPUCLK signal is no longer available in the European TMS9929.



CPU/VDP/VRAM BLOCK DIAGRAM

9900
CPU

TMS 9900 PIN ASSIGNMENTS



NSAG

9918-9928-9929
VDP

TMS 9918 TEST PROGRAM

9928/29

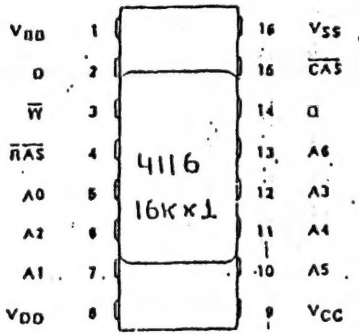
TYPE	PIN		PIN	TYPE
OUT	RAS	1	40	XTAL1 IN
OUT	CAS	2	39	XTAL2 IN
OUT	AD7	3	38 P-Y	CCLK OUT
OUT	AD6	4	37	CCLK OUT
OUT	AD5	5	36 Y	CVID OUT
OUT	AD4	6	35 B-Y	XVID IN
OUT	AD3	7	34	RSET/SYN IN
OUT	AD2	8	33	VCC PWR
OUT	AD1	9	32	RD0 IN
OUT	AD0	10	31	RD1 IN
OUT	R/W	11	30	RD2 IN
PWR	VSS	12	29	RD3 IN
IN	MODE	13	28	RD4 IN
IN	CSW	14	27	RD5 IN
IN	CSR	15	26	RD6 IN
OUT	INT	16	25	RD7 IN
I/O	CD7	17	24	CD0 I/O
I/O	CD6	18	23	CD1 I/O
I/O	CD5	19	22	CD2 I/O
I/O	CD4	20	21	CD3 I/O

NSAG

4116
VRAM

PIN NAMES

A0 A5	Address inputs
CAS	Column address strobe
D	Data input
DATA OUT	Data output
RAS	Row address strobe
S	Chip select
W	Write enable
VBB	−5 V power supply
VCC	+5 V power supply
VDD	+12 V power supply
VSS	0 V ground



- DYN
- SIN CY STO
- 300 PAC
- ZIN REF
- 0°

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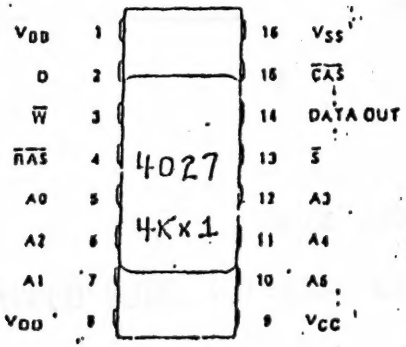

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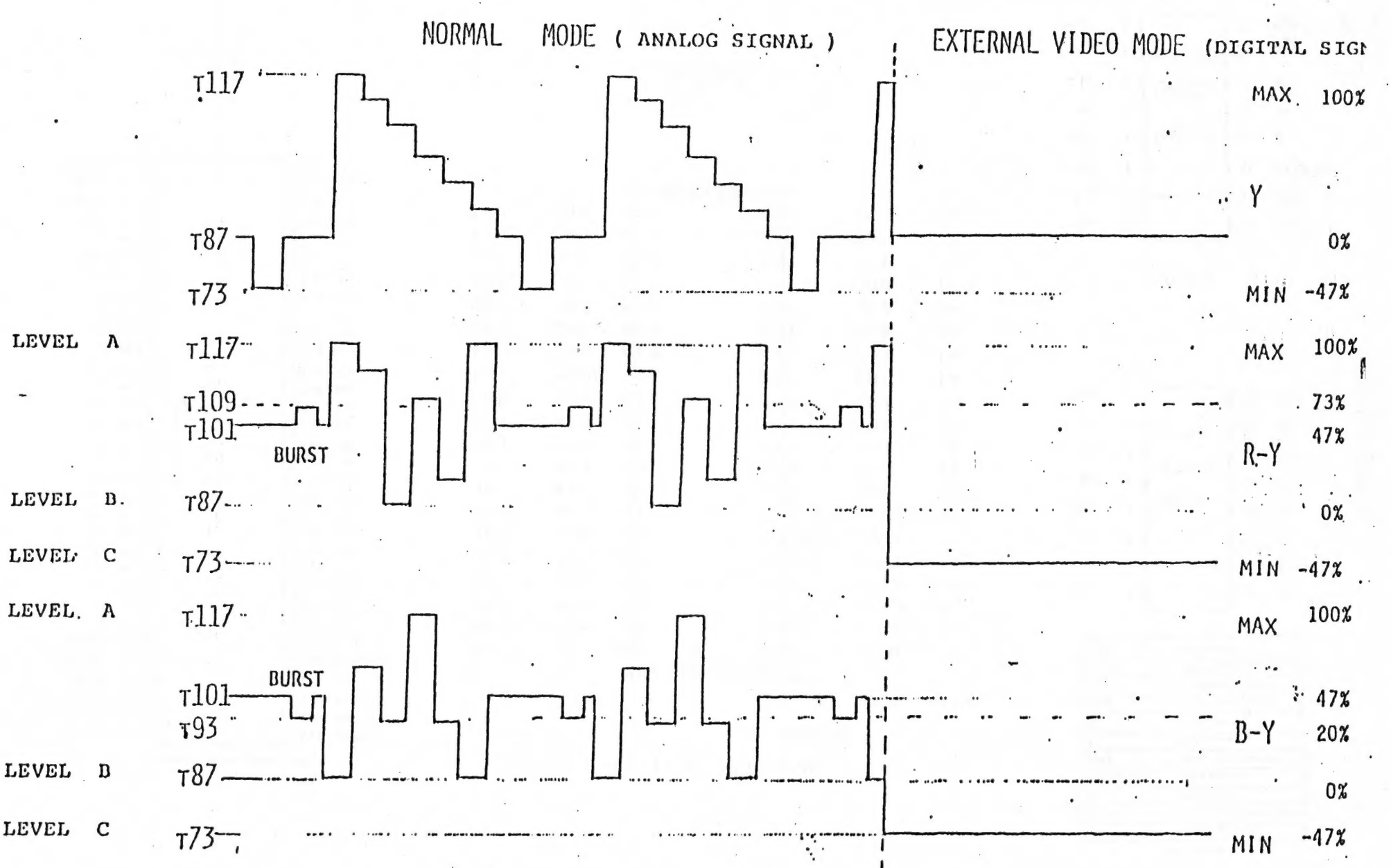

% Indicates percentage of black-white (T117-T87) swing

9928 SIGNAL WAVEFORMS

(AT 5 VOLTS)

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VERTICAL LINE ASSIGNMENT
EURO-VDP 9928

LOCATION	NAME	
LINE 001-052	TOP BORDER	52
LINE 053-244	ACTIVE AREA	192
LINE 245-295	BOTTOM BORDER	~~51~~ 50 (FOR 313 LINES)
LINE 296-298	VERTICAL FRONT BLANKING	3
LINE 299-301	VERTICAL SYNC	3
LINE 302-314	VERTICAL BACK BLANKING	13
	LINE TOTAL	314

THE VERTICAL TO HORIZONTAL ASPECT RATIO WILL BE

VERT:HORIZONTAL = 192:256 OR 3:4

ALL OTHER VERTICAL LINES AND HORIZONTAL COUNTS ARE USED FOR BLANKING, BORDER OR SYNC.

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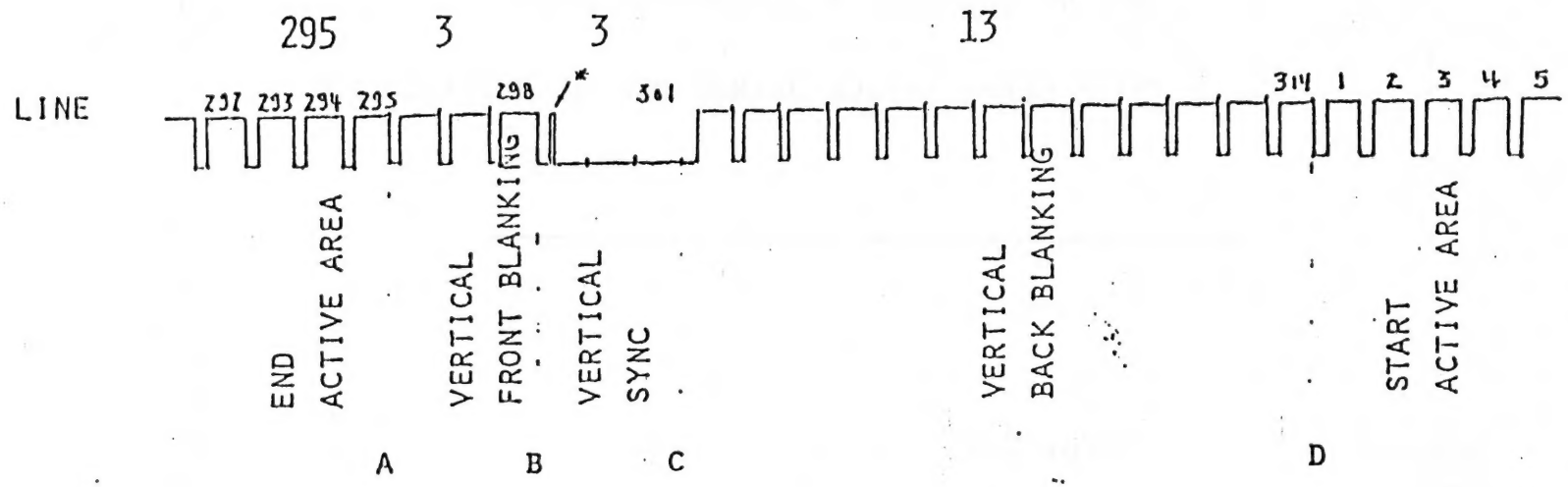
9928 PAL/SECAM VERTICAL TIMING



NAME	LOCATION	LINE COUNTS	TIME
ACTIVE + BORDER AREA	D-A	295	18.79MSEC
VERT. FRONT BLANKING	A-B	3	191.09USEC
VERTICAL SYNC	B-C	3	191.09USEC
VERT.BACK BLANKING	C-D	13	828.04USEC
TOTAL BLANKING	A-D	19	1.21MSEC
TOTAL LINES	A-A	314	20MSEC

ONE LINE DURATION 63.695USEC

MODE OF OPERATION IS NON-INTERLACED

* 465 NSEC DURATION PULSE

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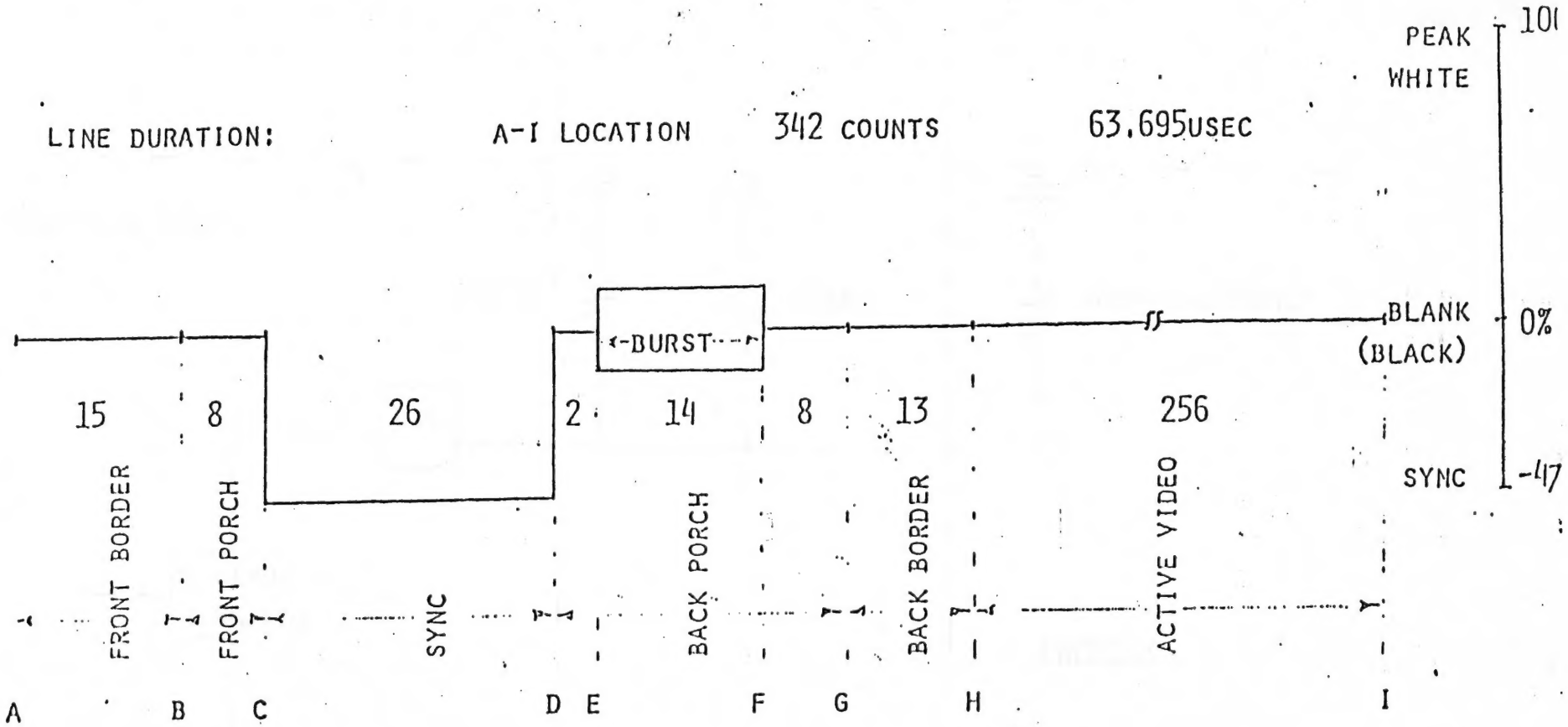
9928 PAL VDP HORIZONTAL TIMING

LINE DURATION: A-I LOCATION 342 COUNTS 63.695USEC



NAME	LOCATION	COUNTS *	TIME(USEC)
FRONT PORCH	B-C	8	1.49
SYNC	C-D	26	4.84
BACK PORCH	D-G	24	4.47
BURST	E-F	14	2.6
BLANKING	B-G	58	10.8
FRONT BORDER	A-B	15	2.8
BACK BORDER	G-H	13	2.42
ACTIVE AREA	H-I	256	47.67

* COUNT = 186.24NSEC

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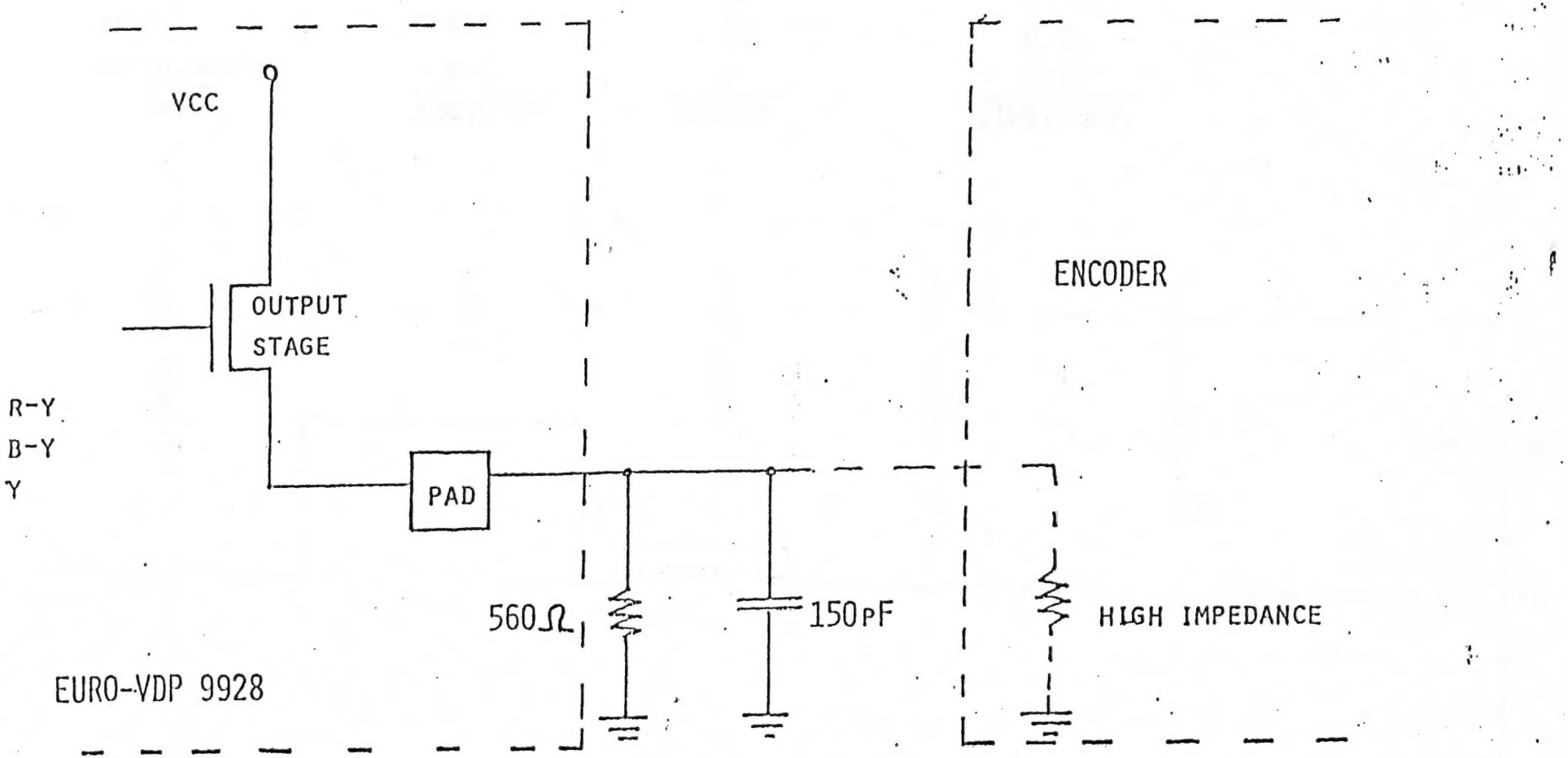
TYPICAL R-Y, B-Y, Y OUTPUT INTERFACE WITH ENCODER



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VBB = -3v Always

			TEMPERATURE (JUNCTION)		0°C		110°C	
			POWER SUPPLY (VOLTS)		4.5	5.5	4.5	5.5
Y	WHITE	(117)			2.35	4.04	2.32	4.00
	BLACK	(87)			1.47	2.85	1.45	2.84
	SYNC	(73)			1.07	2.30	1.06	2.30
R-Y	MAX	(115)			2.29	3.96	2.23	3.92
	MIN	(87)			1.47	2.85	1.45	2.84
	MONOCHROME	(101)			1.88	3.40	1.84	3.38
	EXT. VID.	(73)			1.07	2.30	1.06	2.30
B-Y	MAX	(117)			2.35	4.04	2.32	4.00
	MIN	(89)			1.53	2.93	1.50	2.92
	MONOCHROME	(101)			1.88	3.40	1.84	3.38
	EXT. VID.	(73)			1.07	2.30	1.06	2.30
Y - SWING (WHITE-SYNC)					1.28	1.74	1.26	1.76
R-Y SWING					.82	1.11	.79	1.08
B-Y SWING					.82	1.11	.82	1.08

OUTPUT VOLTAGES 9929
SIMULATED USING 560 OHM PULL-DOWN

9928/9929 signal amplitudes
as percentage of black-white amplitude swing

COLOR CODE	COLOR	Y	R-Y	B-Y
F	WHITE	1.00	.47	.47
E	GRAY	.8	.47	.47
D	MAGENTA	.53	.73	.67
C	GREEN 3	.47	.13	.23
B	YELLOW 1	.8	.6 .57	.17
A	YELLOW 2	.73	.6 .57	.07
9	RED 1	.67	.93	.27
8	RED 2	.53	.93	.27
7	CYAN	.73	0.0	.7
6	RED 3	.47	.83	.3
5	BLUE 1	.53	.43	.93
4	BLUE 2	.4	.4	1.00
3	GREEN 1	.67	.17	.27
2	GREEN 2	.53	.07	.2
1	BLACK/BLNK	0.0	.47	.47
0	TRANSPAR.	---	---	---
SYNC	NONE	-.46	.47 28A	.47 28A
BURST	NONE	0.0	.73 .47	.2 .10
EXT.VIDEO	NONE	0.0	-.46 -.47	-.46 -.47

Prepared by: Carlo Herrmann

Ext. : 82-3520 ; MS :5713

Lubbock

6.0 TMS 9918 Electrical Specifications

6.1 Absolute maximum rating over operating free-air temperature range (unless otherwise noted)*.

Supply Voltage, Vcc (See note 1)	-0.3V to 20V
All Input and Output Voltages	-0.3V to 20V
Continuous Power Dissipation	1.8W
Operating Free-Air Temperature Range	0°C to 55°C
Storage Temperature Range	-55°C to 150°C

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-conditions for extended periods may affect device reliability.

Note 1: Unless otherwise noted, all voltages are with respect to Vss.

.2 Recommended Operation Conditions

	MIN	NOM	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Supply Voltage, V_{SS}		0		V
High Level Input Voltage, V_{IH} All pins except reset	2.2			V
Low level Input Voltage, V_{IL} All Pins			0.8	V
High level Input Voltage Reset, V_{IHR}	3.0			V
Sync Level Input Voltage Reset, V_{IHS}	10.0			V
Operating Free-Air Temperature	0		55	^0C

6.3 Electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted).

PARAMETERS		TEST CONDITIONS	MIN	TYP*	MAX	UNITS
I_i	Input Leakage Current	V_i=0V to V_{cc} All other pins=0V			±10	uA
I_o	Tristate Leakage Current D_0 - D7	V_i=0V to V_{cc}			±100	uA
V_{OH}	High Level Output Voltage	I_{oh}= -400 uA	2.4			V
V_{OL}	Low Level Output Voltage For CPU Data	I_{OL}=1.2 mA			.4	V
V_{OLM}	Low Level Output Voltage For DRAM I/F	I_{OL} = 800 uA			.4	V
V_{OHS}	High Level Output Voltage for $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$		2.7			V
V_W	Video Voltage Level of White	V_{cc}=5V		3.2		V
V_{VB}	Video Voltage Level of Black (blank)	V_{cc}=5V		2.3		V
V_{VS}	Video Voltage Level of Sync	V_{cc}=5V		1.9		V
V_{VBA}	Video Voltage Peak to Peak of Burst	V_{cc}=5V		.5		V
V_{VR}	Video Range (White-Black)		.5			V
I_{CC}	Supply Current From V_{cc}	TA = 25°C		200	250	mA
C_i	Input Capacitance	F = 1MHz unmeasured pins at V_{ss}			10	pf
D_0-D_7	Data I/O Capacitance	F = 1MHz unmeasured pins at V_{ss}			20	pf
C_o	Output Capacitance	F = 1MHz unmeasured pins at V_{ss}			20	pf

* All typical values are at T_a = 25°C and nominal voltages.

4 Timing requirements over recommended supply voltage range and operating free-air temperature range.

CPU - VDP Interface

Parameters		MIN	TYP	MAX	UNITS
t_{ASRL}	Address set up time before $\overline{CSR}$ low	0			NS
t_{ASWL}	Address set up time before $\overline{CSW}$ low	50			NS
t_{AHWL}	Address hold time after $\overline{CSW}$ low	50			NS
t_{CSWW}	$\overline{CSW}$ pulse width, low	220			NS
t_{DSWH}	Data set up time before $\overline{CSW}$ high	50			NS
t_{CACM}	Chip select high requesting memory access until next chip select low	8			uS
t_{DHWH}	Data hold time after $\overline{CSW}$ high	50			NS
t_{CACV}	Chip select high not request memory access until next chip select low	3			uS
t_{AHRH}	Address hold time after $\overline{CSR}$ high	0			NS

VDP - VRAM Interface

t_{ct}	Memory read or write cycle time	372			NS
$t_a(C)$	Data access time from $\overline{CAS}$			150	NS
$t_a(R)$	Data access time from $\overline{RAS}$			200	NS
t_{su}(DATA)	Input data set up time before $\overline{CAS}$ low	100			NS
t_h (DATA)	Input data hold time after $\overline{CAS}$ low	0			NS

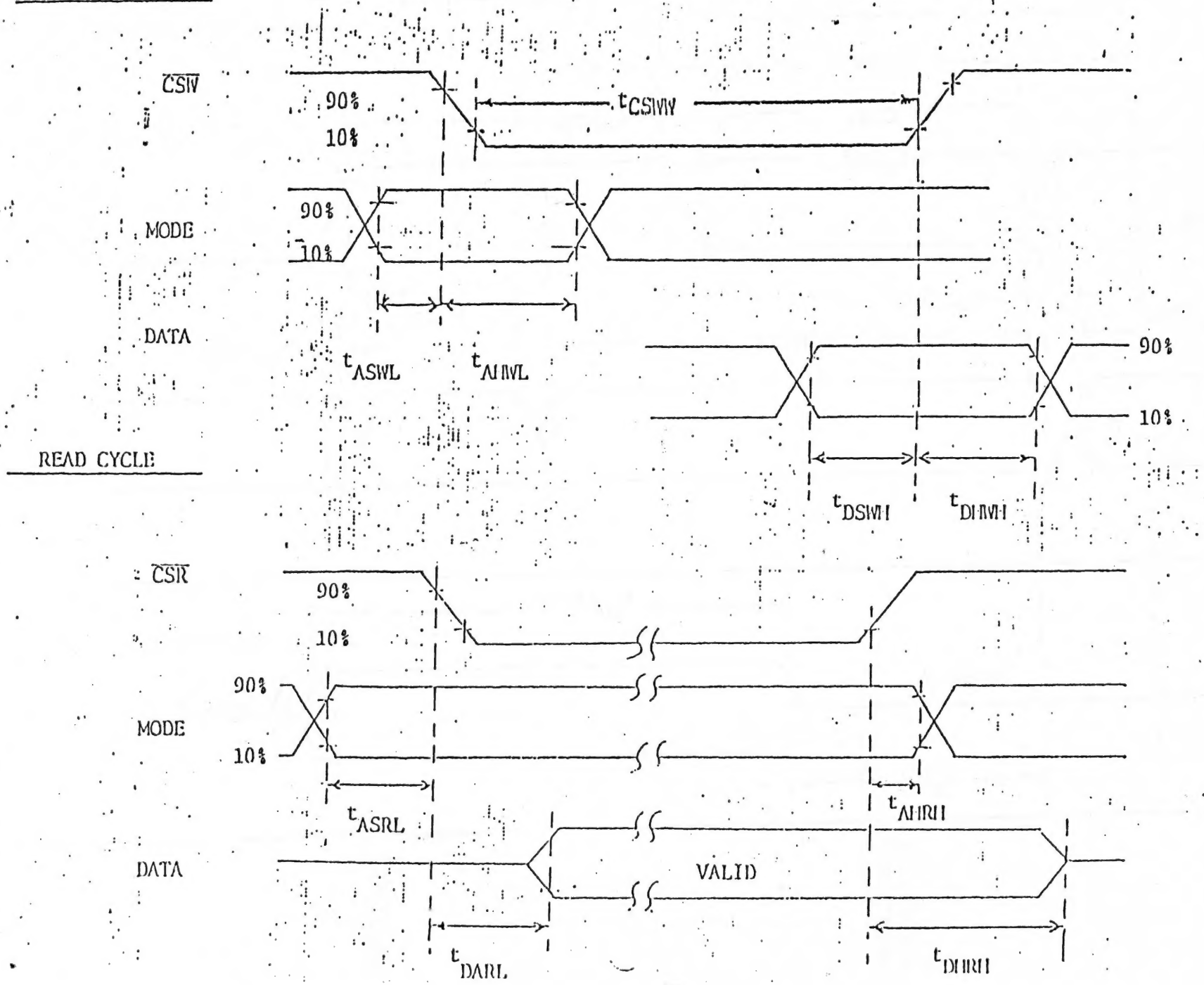
6.5 Switching Characteristics over full range of recommended operating conditions.

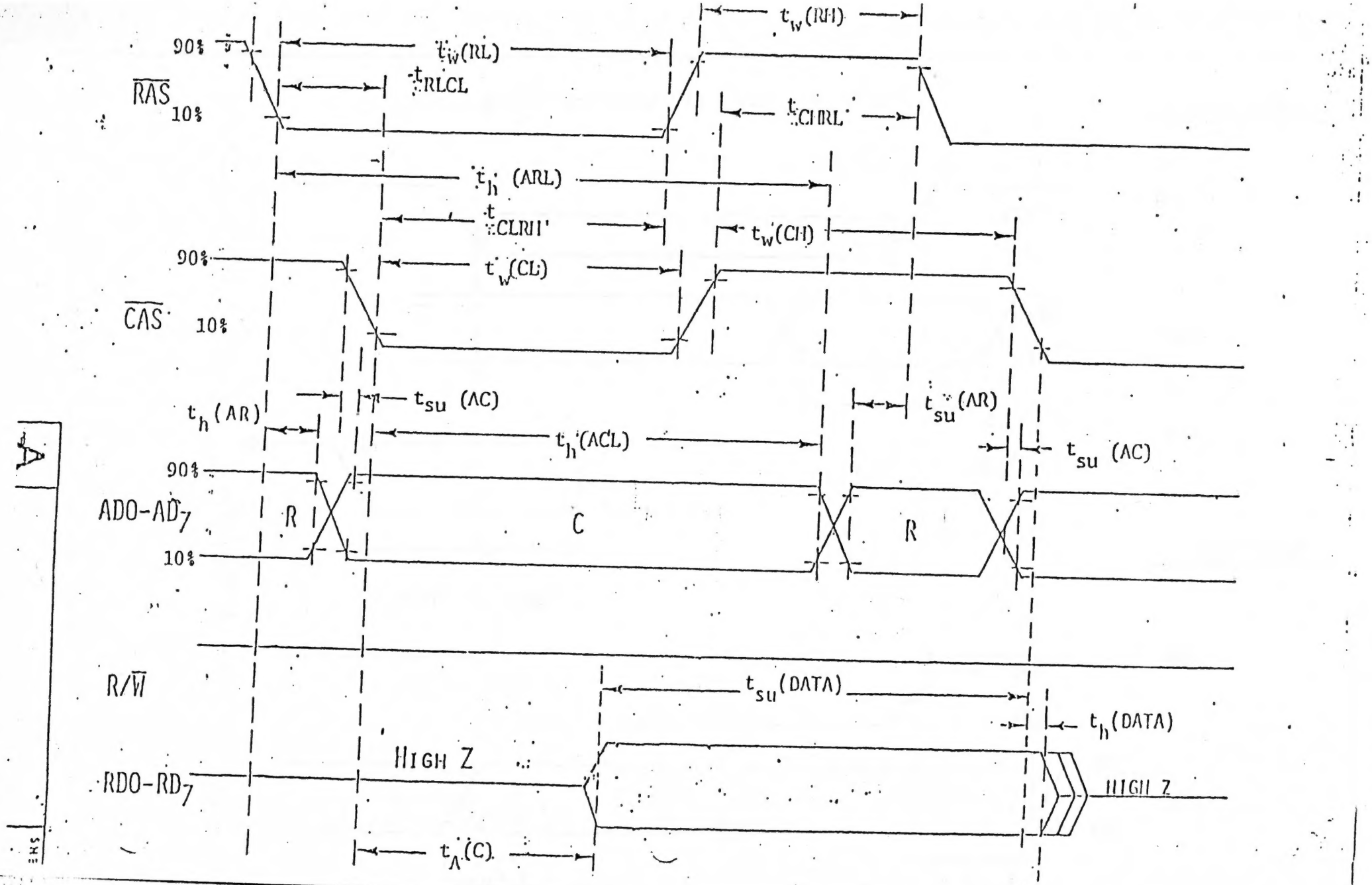
Parameters		TEST COND	MIN	TYP	MAX	UNITS
CPU - VDP Interface						
t_{DARL}	Data access time from $\overline{CSR}$	C_L=300pf			400	NS
t_{DHRH}	Data hold time from $\overline{CSR}$ high	C_L=300pf	0		300	NS
CPU-Clock	÷3 Output Clock			3.58		MH_z
GROM-Clock	÷24 Output Clock			447.5		KH_z
VDP - VRAM Interface						
t_w(CH)	Pulse width, column address strobe high		150			NS
t_w(CL)	Pulse width, column address strobe low		150			NS
t_w(RH)	Pulse width, row address strobe high		120			NS
t_w(RL)	Pulse width, row address strobe low		200			NS
t_w(W)	Write pulse width low		150			NS
t_{su}(AC)	Column address set up time		-20			NS
t_{su}(AR)	Row address set up time		10			NS
t_{su}(D)	Data set up time		-15			NS
t_{su}(rd)	Read command set up Time		50			NS
t_{su}(WCH)	Write command set up time before $\overline{CAS}$ high		75			NS

(Switching Characteristics, continued)

Parameters		TEST COND	MIN	TYP	MAX	UNITS
$t_{su}(WRH)$	Write command set up time before $\overline{RAS}$ high		75			NS
$t_h(ACL)$	Column address hold time after $\overline{CAS}$ low		60			NS
$t_h(AR)$	Row address hold time		20			NS
$t_h(ARL)$	Column address hold time after $\overline{RAS}$ low		95			NS
$t_h(DCL)$	Data hold time after $\overline{RAS}$ low		240			NS
$t_h(DRL)$	Data hold time after $\overline{RAS}$ low		280			NS
$t_h(DWL)$	Data hold time after $\overline{W}$ low		145			NS
$t_h(rd)$	Read command hold time		25			NS
$t_h(WCL)$	Write command hold time after $\overline{CAS}$ low		245			NS
t_{CHRL}	Delay time, column address strobe high to row address strobe low		100			NS
t_{CLRH}	Delay time, column address strobe low to row address strobe high		150			NS
t_{RLCL}	Delay time, row address strobe low to column address strobe low		35			NS

Figure 6-6 VDP - CPU Interface Timing




t_w(RH)
90%
t_w(RL)
t_{RLCL}
RAS
10%
t_{CHRL}
t_h (ARL)
t_{CLRH}
t_w(CH)
90%
t_w(CL)
CAS
10%
t_h (AR)
t_{su} (AC)
t_{su} (AR)
t_h(ACL)
t_{su} (AC)
90%
ADO-AD7
R
C
R
10%
R/W
t_{su}(DATA)
t_h(DATA)
HIGH Z
RDO-RD7
HIGH Z
t_A(C)